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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/063,880	05/21/2002	Kuo-Ming Chen	NAUP0481USA	2347

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EXAMINER	
NGUYEN, DILINH P	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 05/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/063,880	CHEN, KUO-MING	
	Examiner	Art Unit	
	DiLinh Nguyen	2814	

-- The MAILING DATE of this communication appears on the cover she t with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-26 and 28-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-26 and 28-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1, 5-7, 16 are rejected under 35 U.S.C. 102(a) as being anticipated by Ishii (J.P. 2001-257289).

- Regarding claims 1 and 6, Ishii discloses a semiconductor device (figs. 7a-7b) comprising:

  a substrate 1;

  solder pads with two sizes of diameters;

  a plurality of first solder pads 2d positioned on a surface of the substrate, each of the first solder pads having a first diameter; and

  at least a second solder pad 2a positioned on a corner region of the substrate surface, the second solder pad having a second diameter greater than the first diameter. Since Ishii discloses all claimed structure features. Therefore, the package inherently sustains a stronger thermal stress, a high stress region and a stronger fatigue strength.

- Regarding claim 5, Ishii discloses the substrate 1 comprises a chip (figs. 7a-7b).
- Regarding claim 7, Ishii discloses the first solder pads are arranged in a matrix at a center region of the substrate.

- Regarding claim 16, Ishii discloses each of the first solder pad and the second solder pad comprise a solder ball pad 8a/8dd, the solder ball pad connecting to a solder ball to connect to a board 7 (figs. 9a-9b).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 2-4 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishii in view of Guzuk et al. (U.S. Pat. 5153379).

Ishii discloses the claimed invention except for not specifically point out that the substrate comprises a plastic substrate or a ceramic substrate.

Guzuk et al. disclose a semiconductor device comprising a substrate and wherein the substrate is preferably a ceramic board, an insulating material such as glass epoxy board or a printed circuit board (column 2, lines 39-45). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Ishii to increase the heat dissipating characteristics, as shown by Guzuk et al.

- Regarding claim 13, Guzuk et al. disclose the corner region comprises at least a grounded solder pad (column 1, lines 66-67 and column 2, lines 5-6).

3. Claims 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishii in view of Applicant Admitted Prior Art (figs. 1 and 4).

- Regarding claim 9, Ishii discloses the claimed invention except for not specifically point out that the corner region comprises the circumferences of a plurality of concentric circles on the susbstrate.

AAPA (fig. 4) disclose a plurality of first solder pads 14 and a plurality of second solder pads 24, the plurality of second solder pads 24 positioned on a corner region; wherein the corner region comprises the circumferences of a plurality of concentric circles on the substrate. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Ishii to prevent the package not crack easily at the corner of the chip.

- Regarding claim 10, AAPA discloses the second solder pads on each of the concentric circle circumferences are arranged with an equal interval.
- Regarding claim 11, AAPA discloses the corner region comprises the corners of the substrate on an outside portion of a maximum circle on the substrate.
- Regarding claim 12, AAPA discloses the corner region comprises the circumference of a maximum circle on the substrate.

4. Claims 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishii in view of Capote et al. (U.S. Pat. 6518677).

Ishii fails to disclose a solder bump pad and solder bumps and using the solder bump to connect to a chip.

Capote et al. disclose a semiconductor device comprising: plurality of solder pads 12 comprise a solder bump pad 24, the solder bump pad connecting to a solder bump 14 and using the solder bump to connect to a chip 10. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Ishii to provide a direct electrical connection through bumps reduces signal transmission path and high packaging density, as shown by Capote et al.

- Regarding claim 15, Capote et al. disclose an underfill layer 22 is filled in a gap between the chip and the substrate.

5. Claims 17, 20-22 and 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pu et al. (U.S. Pat. 6350669) in view of Ishii.

Pu et al. discloses a semiconductor device (cover fig.) comprising:

a substrate 310;

a plurality of first solder bump pads A2 positioned on a first surface of the substrate, each of the first solder bump pads having a first diameter and

at least a second solder bump pad A1 positioned on a first predetermined region of the first surface, the second solder bump pad having a second diameter greater than the first diameter (column 4, lines 52-54), each of the first solder bump pads and the second solder bump pad being connected to a solder bump 321 that is connected to a chip 300.

Pu et al. fail to disclose a plurality of first solder ball pads positioned on a second surface of the substrate, each of the first solder ball pads having a third diameter, and at

least a second solder ball pad positioned on a second predetermined region of the second surface, the second solder ball pad having a second diameter greater than the third diameter.

Ishii discloses a semiconductor device (figs. 7a-b) comprising:

a plurality of first solder ball pads 2d positioned on a second surface of the substrate 1, each of the first solder ball pads having a third diameter; and

at least a second solder ball pad 2a positioned on a second predetermined region of the second surface, the second solder ball pad having a fourth diameter greater than the third diameter, each of the first solder ball pads and the second solder ball pad being connected to a solder ball 3 that is connected a circuit board 7 (figs. 9a-b). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Pu et al. to provide a high reliability for the semiconductor package device and relax the influence of distortion caused by difference in thermal expansion between the package and the mounting board, as shown by Ishii.

- Regarding claim 20, since Pu et al. and Ishii disclose all claimed structural features. Therefore, the package inherently comprises a high stress region at the first predetermined region and the second predetermined region.
- Regarding claims 21 and 28, Ishii discloses the small diameter pads are arranged in a matrix at a center region of the substrate.
- Regarding claims 22 and 29, Ishii discloses the predetermined region compries the corners on the surface of the substrate.

6. Claims 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pu et al. (U.S. Pat. 6350669) in view of Ishii and further in view of Guzuk et al.

Pu et al. and Ishii discloses the claimed invention except for not specifically point out that the substrate comprises a plastic substrate or a ceramic substrate.

Guzuk et al. disclose a semiconductor device comprising a substrate and wherein the substrate is preferably a ceramic board, an insulating material such as glass epoxy board (column 2, lines 39-45). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Pu et al. and Ishii to increase the heat dissipating characteristics, as shown by Guzuk et al.

7. Claims 18-19, 23-26 and 30-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pu et al. in view of Ishii and further in view of Applicant Admitted Prior Art (figs. 1 and 4).

- Regarding claims 23 and 30, Pu et al. and Ishii disclose the claimed invention except for not specifically point out that the predetermined region comprises the circumferences of a plurality of concentric circles on the substrate.

AAPA (fig. 4) disclose a plurality of first pads 14 and a plurality of second pads 24, the plurality of second pads 24 positioned on a predetermined region; wherein the predetermined region comprises the circumferences of a plurality of concentric circles on the substrate. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Pu et al. and Ishii to prevent the package not crack easily at the corner of the chip.

- Regarding claims 18-19, AAPA (fig. 1) disclose a substrate 18 comprises a plastic substrate or a ceramic substrate.
- Regarding claims 24 and 31, AAPA discloses the second pads on each of the concentric circle circumferences are arranged with an equal interval.
- Regarding claims 25 and 32, AAPA discloses the predetermined region comprises the corners of the substrate on an outside portion of a maximum circle on the substrate.
- Regarding claims 26 and 33, AAPA discloses the predetermined region comprises the circumference of a maximum circle on the substrate.

Response to Arguments

Applicant's arguments with respect to claims 1-7, 9-26 and 28-33 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DiLinh Nguyen whose telephone number is (571) 272-1712. The examiner can normally be reached on 8:00AM - 6:00PM (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DLN

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